

## General Description

The Sanrise SRT04N016L is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT04N016L break down voltage is 40V and it has a high rugged avalanche characteristics. The SRT04N016L is available in PDFN5\*6 package.

## Features

- Ultra Low  $R_{DS(ON\_TYP)} = 1.15m\Omega @ V_{GS} = 10V$ .
- Ultra Low Gate Charge,  $Q_g = 85nC$  typ.
- Fast switching capability
- Robust design with better EAS performance
- EMI Improved
- Non-automotive Qualified

## Application

- Server/Telecom
- High Power Supply
- E-Tools
- BMS

## Symbol

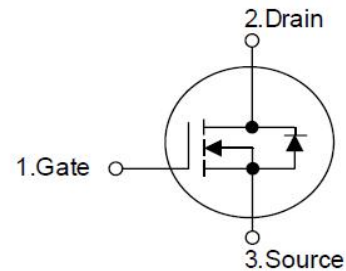
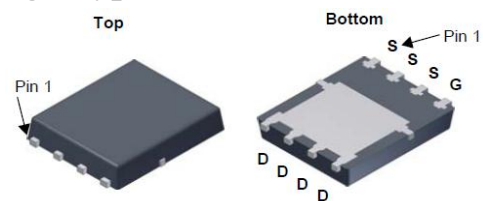


Figure 1 Symbol of SRT04N016L

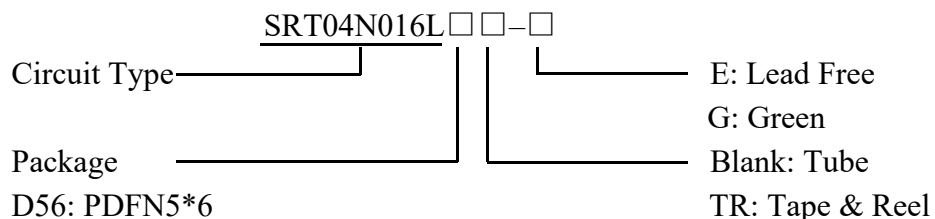
## Package Type



PDFN5\*6

Figure 2 Package Type of SRT04N016L

## Ordering Information



Package	Part Number		Marking ID		Packing Type
	Lead Free	Green	Lead Free	Green	
PDFN5*6	SRT04N016LD56TR-E	SRT04N016LD56TR-G	SRT04N016LD56E	SRT04N016LD56G	Tape & Reel

**Absolute Maximum Ratings**

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		$V_{DSS}$	40	V
Gate-Source Voltage		$V_{GSS}$	±20	V
Continuous Drain Current, Package Limited	$T_C=25^{\circ}C$	$I_D$	100	A
	$T_C=100^{\circ}C$		100	
	$T_C=125^{\circ}C$		77	
Continuous Drain Current, Silicon	$T_C=25^{\circ}C$		173	
Pulsed Drain Current (Note 2)		$I_{DM}$	692	A
Avalanche Energy, Single Pulse (Note 3)		$E_{AS}$	100	mJ
Avalanche Destructive Energy, Single Pulse (Note 4)		$E_{AS\_Limit}$	756	mJ
Avalanche Energy, Repetitive (Note 2)		$E_{AR}$	0.2	mJ
Avalanche Current, Repetitive (Note 2)		$I_{AR}$	50.0	A
Continuous Diode Forward Current		$I_S$	173	A
Diode Pulse Current		$I_{S,PULSE}$	692	A
Max Power Dissipation		$P_D$	100	W
Operating Junction Temperature		$T_J$	150	°C
Storage Temperature		$T_{STG}$	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)		$T_{LEAD}$	260	°C

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3.  $I_{AS} = 20A$ ,  $V_{DD} = 20V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}C$
4.  $I_{AS\_Limit} = 55A$ ,  $V_{DD} = 20V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}C$

**Thermal Resistance**

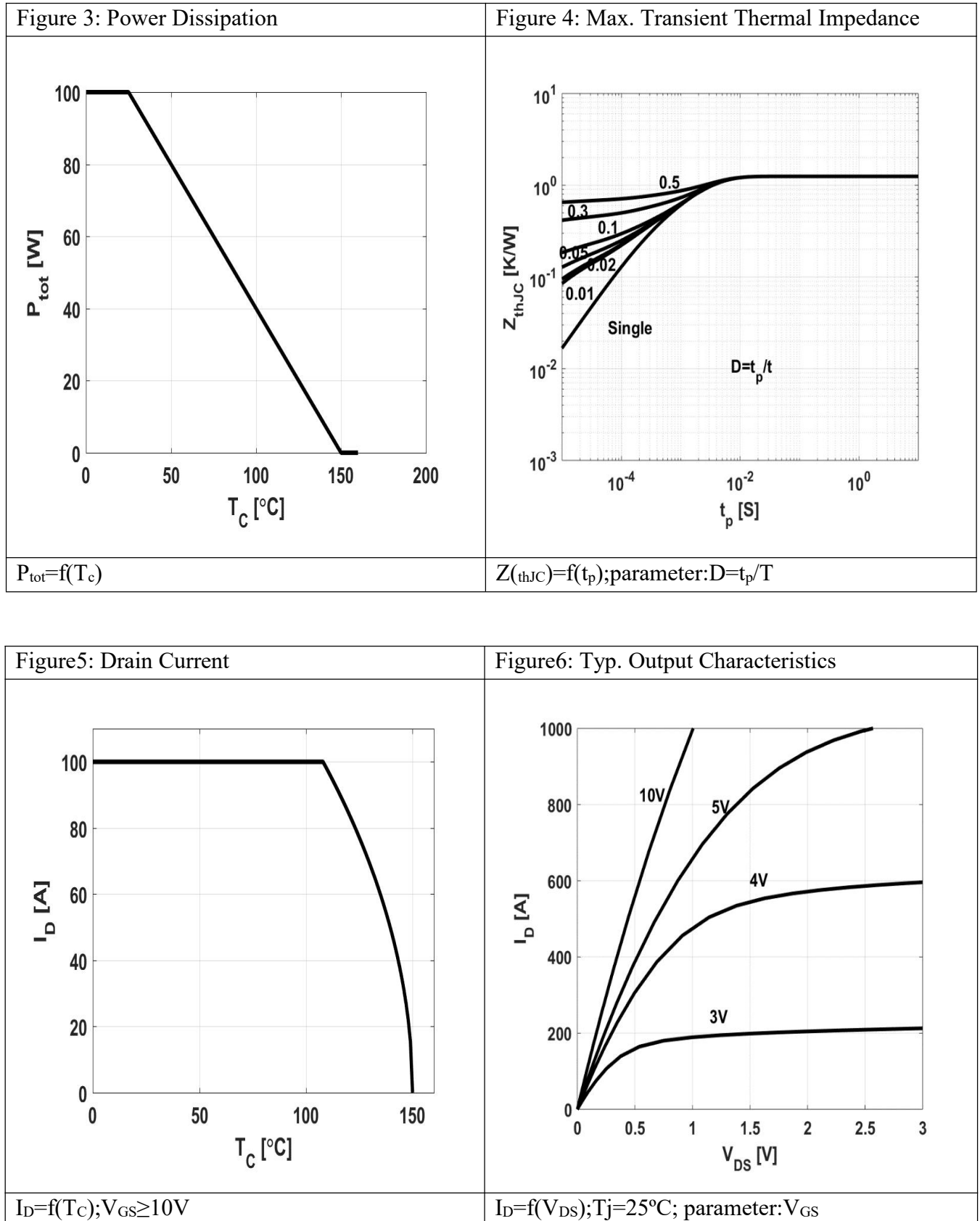
Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	PDFN5*6	$R_{thJC}$			1.2	°C/W
Thermal Resistance, Junction-to-Ambient	PDFN5*6	$R_{thJA}$			50	

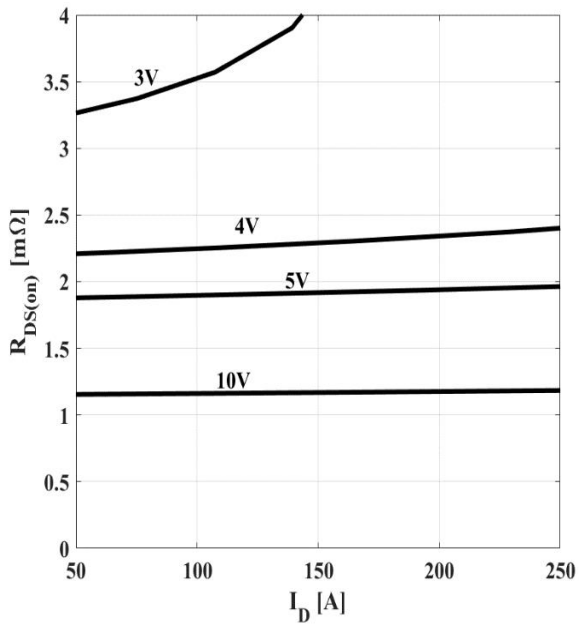
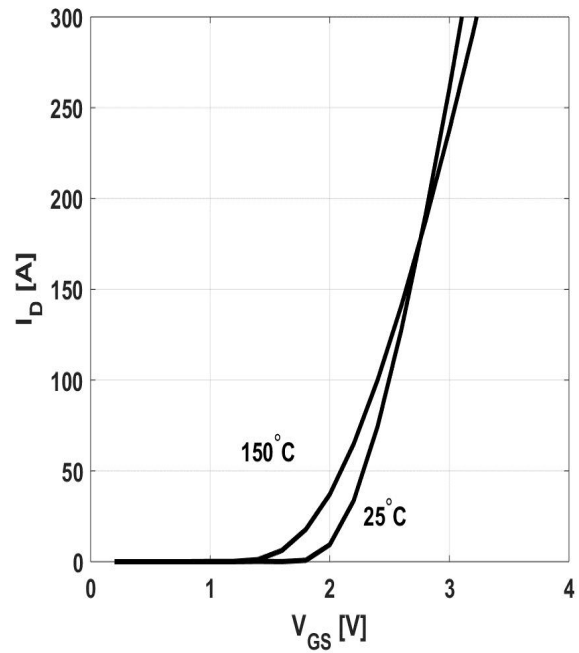
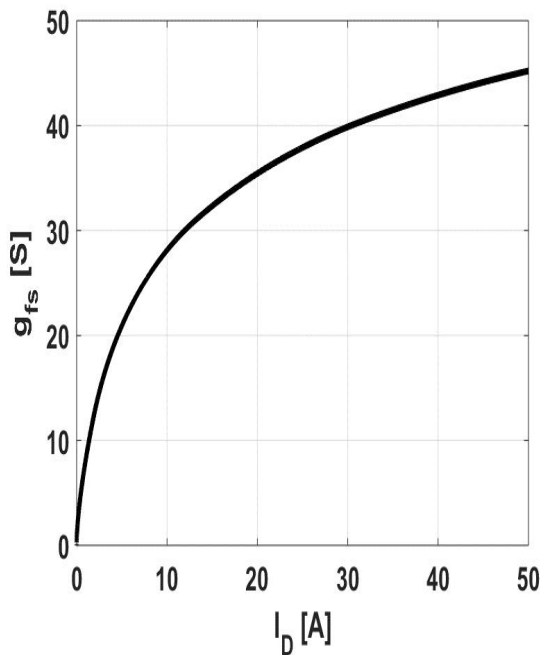
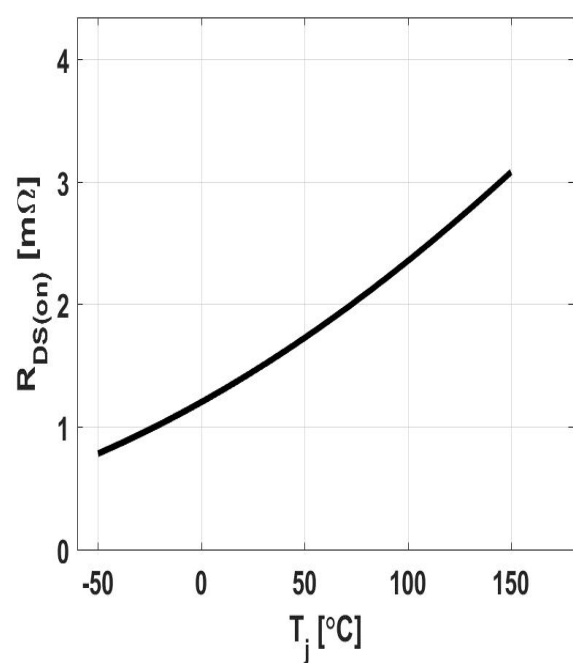
**Electrical Characteristics**
 $T_J = 25^\circ\text{C}$ , unless otherwise specified.

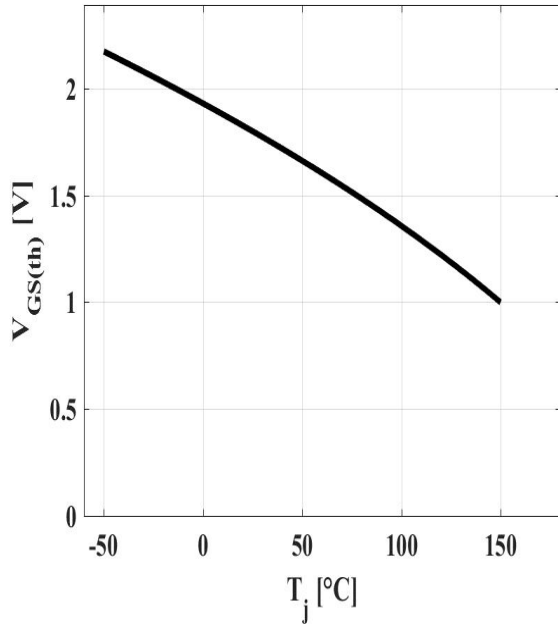
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Statistic Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	Forward	$I_{GSSF}, V_{GS}=20V, V_{DS}=0V$			200	nA
	Reverse	$I_{GSSR}, V_{GS}=-20V, V_{DS}=0V$			-200	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=0.25mA$	1.2	1.8	2.4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=50A$		1.15	1.6	mΩ
		$V_{GS}=4.5V, I_D=50A$		2.0	3.05	
Gate Resistance	$R_G$	$f=1MHz, \text{Open Drain}$		1.3		Ω
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=20V, V_{GS}=0V, f=1MHz$		5.8		nF
Output Capacitance	$C_{OSS}$			1.6		nF
Reverse Transfer Capacitance	$C_{RSS}$			98		pF
Effective output capacitance, energy related <sup>NOTE5</sup>	$C_{O(er)}$	$V_{GS}=0V, V_{DS}=0\dots 32V$		2.4		nF
Effective output capacitance, time related <sup>NOTE6</sup>	$C_{O(tr)}$			3.0		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=50A, R_G=1.6\Omega, V_{GS}=10V$		18		ns
Rise Time	$t_r$			55		
Turn-off Delay Time	$t_{d(off)}$			60		
Fall Time	$t_f$			12		
<b>Gate Charge Characteristics</b>						
Gate to Source Charge	$Q_{gs}$	$V_{DD}=20V, I_D=50A, V_{GS}=0 \text{ to } 10V$		12.5		nC
Gate to Drain Charge	$Q_{gd}$			9.5		
Gate Charge Total	$Q_g$			85		
Gate Plateau Voltage	$V_{plateau}$			2.3		V
Gate Charge Total, sync FET	$Q_g$	$V_{DD}=0.1V, V_{GS}=0 \text{ to } 10V$		79		nC
<b>Reverse Diode Characteristics</b>						
Drain-Source Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_{SD}=50A$		0.84	1.0	V
Reverse Recovery Time	$t_{rr}$	$V_R=400V, I_F=50A, dI_F/dt=100A/\mu s$		60		ns
Reverse Recovery Charge	$Q_{rr}$			120		nC
Peak Reverse Recovery Current	$I_{rrm}$			4.0		A

Note:

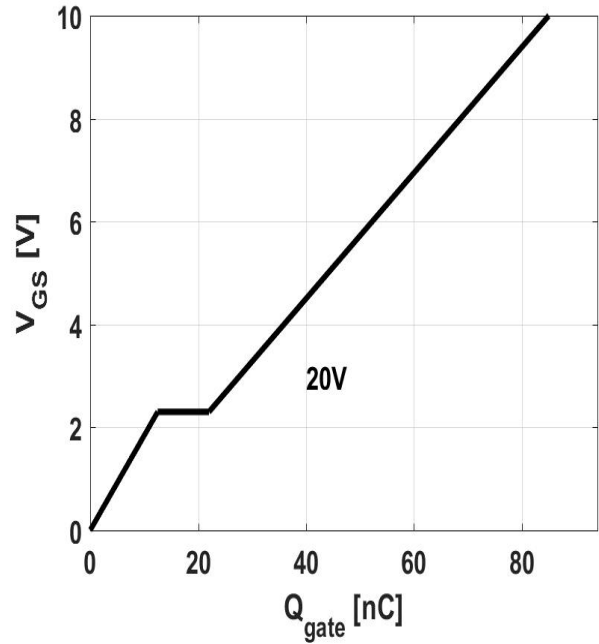
- $C_{O(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 32V
- $C_{O(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 32V

**Typical Performance Characteristics**


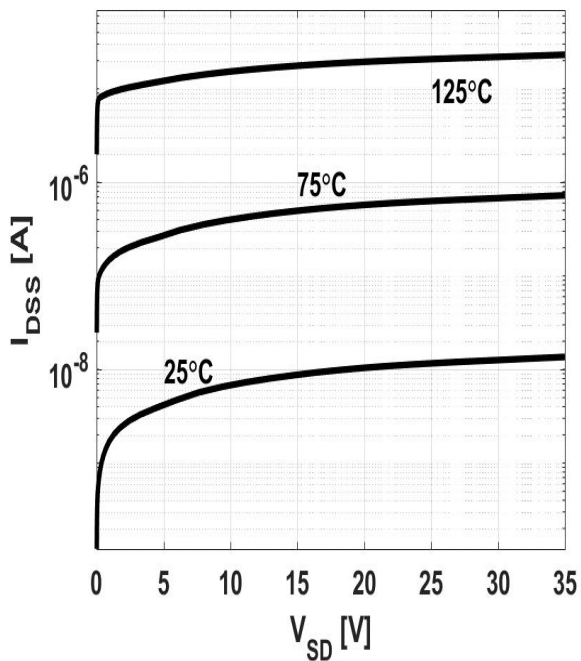
**Figure7: Typ. Drain-Source On-State Resistance**

 $R_{DS(ON)}=f(I_D); T_j=25^\circ C; \text{parameter: } V_{GS}$ 
**Figure8: Typ. Transfer Characteristics**

 $I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}; \text{parameter: } T_j$ 
**Figure9: Typ. Forward Transconductance**

 $g_{fs}=f(I_D); T_j=25^\circ C$ 
**Figure10: Typ. Drain-Source On-State Resistance**

 $R_{DS(ON)}=f(T_j); I_D=50A; V_{GS}=10V$

**Figure 11: Typ. Gate Threshold Voltage**


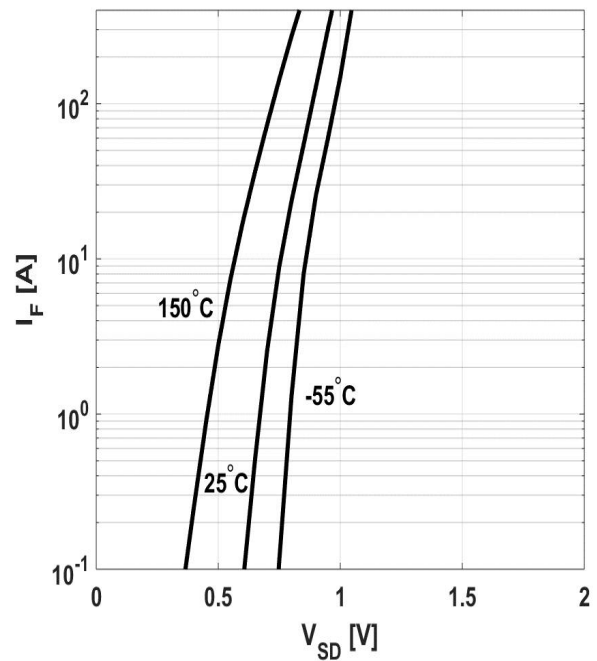
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_{DS} = 250\mu A$$

**Figure 12: Typ. Gate Charge**


$$V_{GS} = f(Q_{gate}), I_D = 50A \text{ pulsed}$$

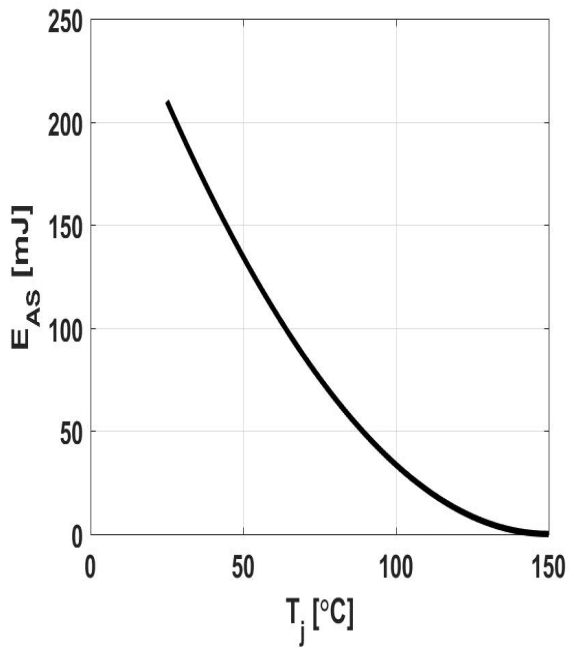
**Figure 13: Drain-Source Leakage Current**


$$I_{DSS} = f(V_{DS}); V_{GS} = 0V; \text{parameter: } T_j$$

**Figure 14: Forward Characteristics of Reverse Diode**


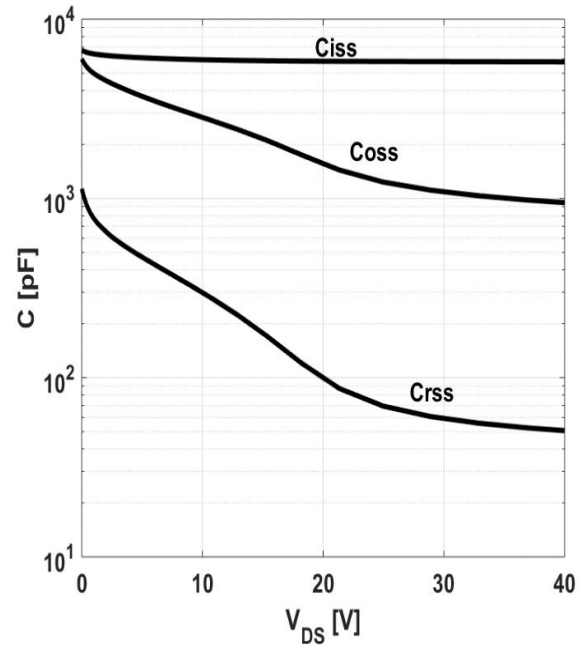
$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Figure 15: Avalanche Energy



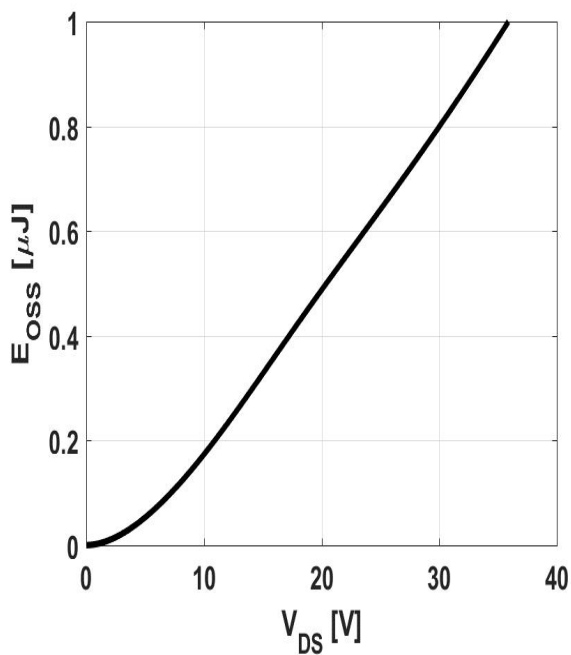
$$E_{AS}=f(T_j); I_D=50.0A; V_{DD}=20V$$

Figure 16: Typ. Capacitances



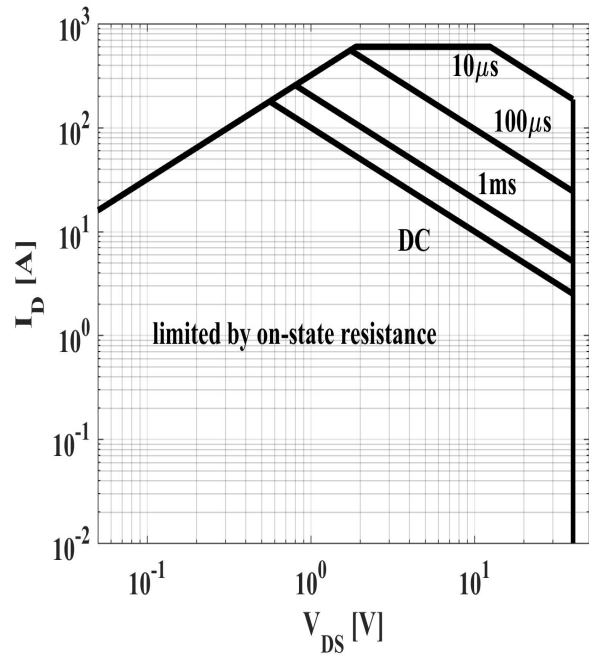
$$C=f(V_{DS}); V_{GS}=0; f=1MHz$$

Figure 17: C\_oss Stored Energy

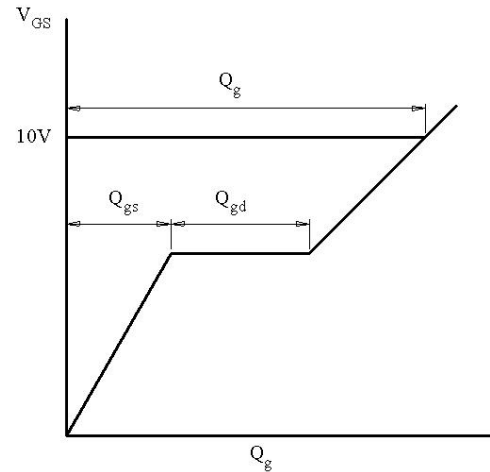
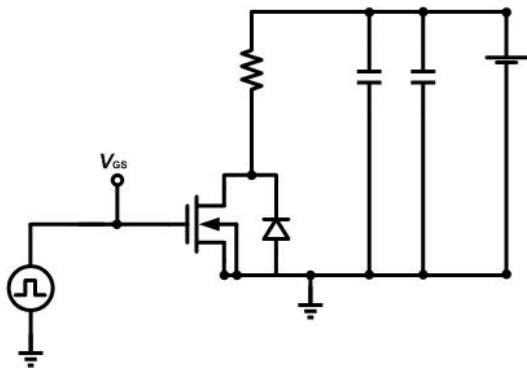
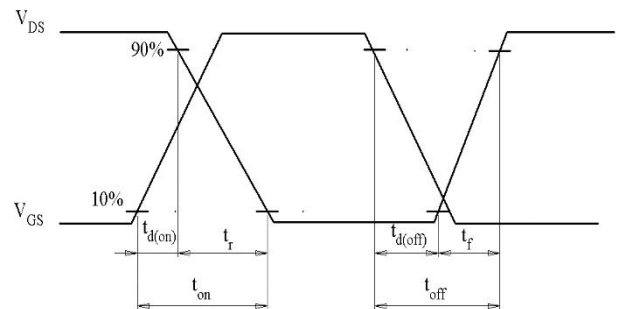
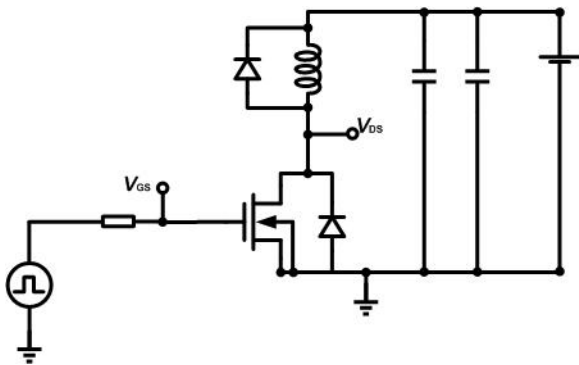
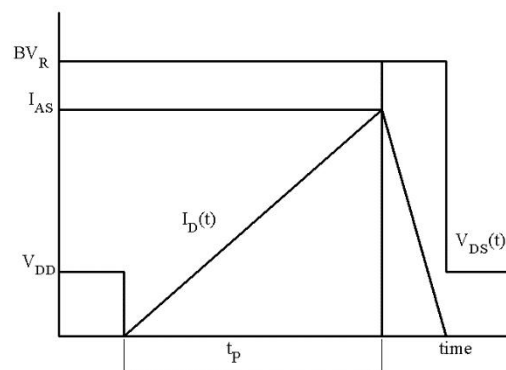
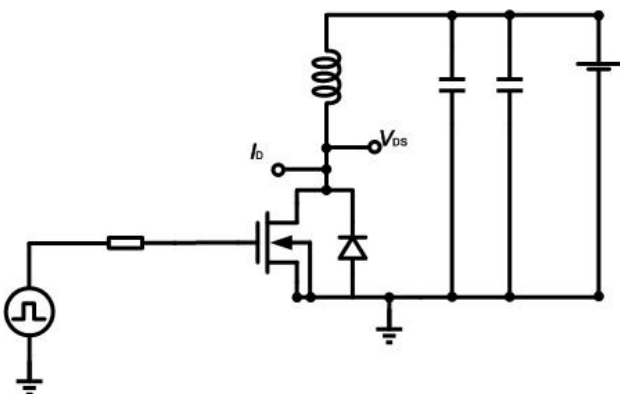


$$E_{OSS}=f(V_{DS})$$

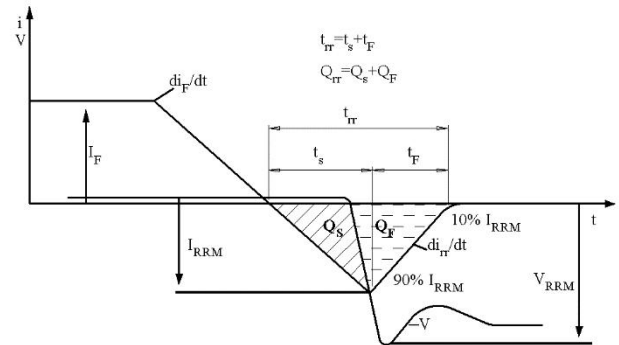
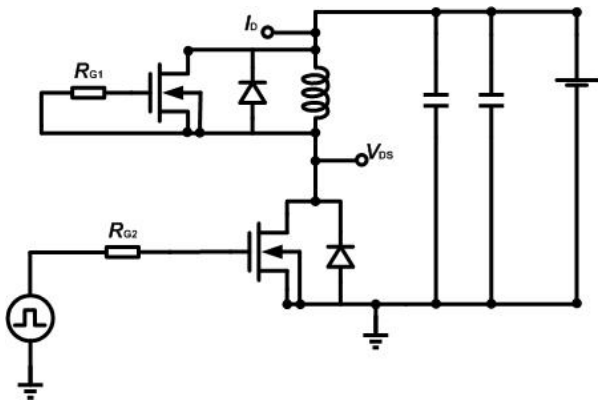
Figure 18: Safe Operating Area

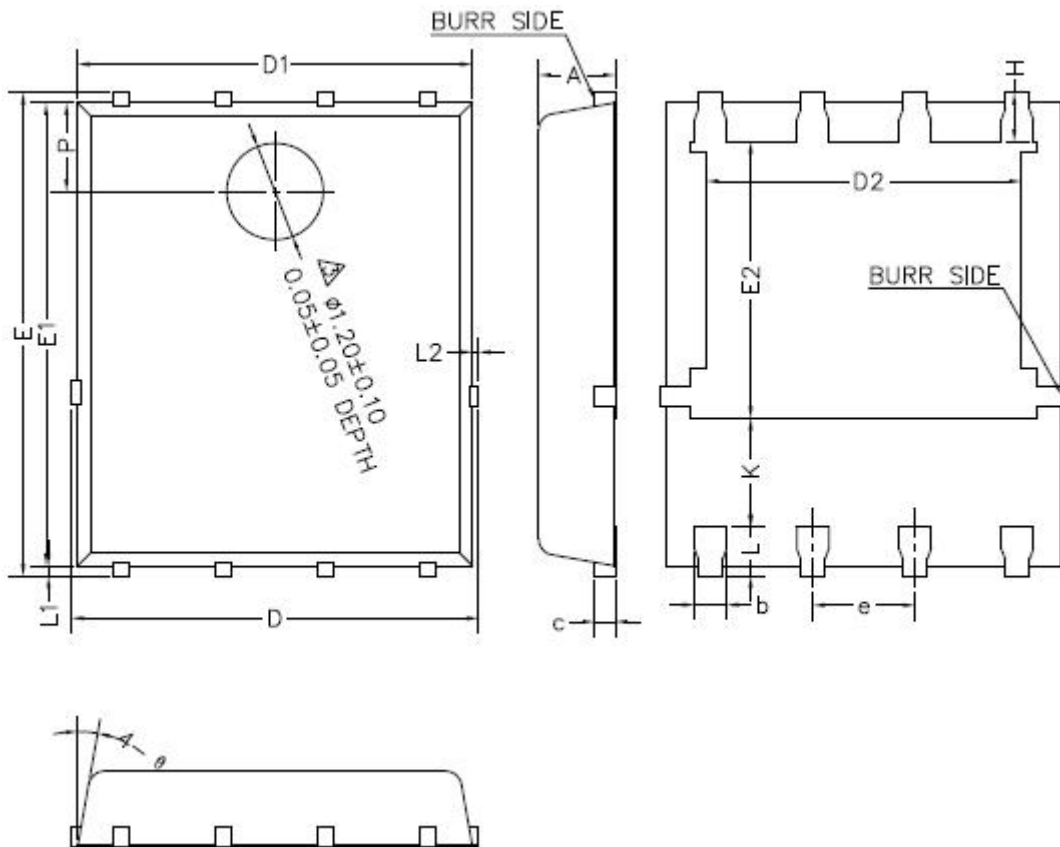


$$I_D = f(V_{DS}); T_c = 25^\circ C; V_{GS} > 7V; \text{parameter } t_p$$

**Test Circuits**
**1. Gate Charge Test Circuit & Waveform**

**2. Switch Time Test Circuit**

**3. Unclamped Inductive Switching Test Circuit & Waveforms**


**4. Test Circuit and Waveform for Diode Characteristics**



**Mechanical Dimensions**
**PDFN5\*6-8 Unit: mm**


Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	1.0	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
$\theta$	8°	10°	12°



Sanrise Technology Limited Company

<http://www.sanrise-tech.com>

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